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L11: Entry 10 of 16

File: USPT

Oct 15, 2002

US-PAT-NO: 6467082

DOCUMENT-IDENTIFIER: US 6467082 B1

TITLE: Methods and apparatus for simulating external linkage points and control transfers in source translation systems

DATE-ISSUED: October 15, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
D'Arcy; Paul Gerard	Alpharetta	GA		
Deschler; Pamela C.	Bethlehem	PA		
Jinturkar; Sanjay	Bethlehem	PA		
Peri; Kamesh	Allentown	PA		
Peri; Ramesh V.	Allentown	PA		
Whalley; David B.	Tallahassee	FL		

US-CL-CURRENT: 717/127; 717/136, 717/163

ABSTRACT:

A method for simulating a first processor (e.g., target processor) on a second processor (e.g., host processor) includes translating assembly language instructions associated with the first processor into `C` language code. The `C` language code is then compiled by a compiler program running on the second processor. The compiled code is then executed by the second processor to simulate the first processor. For example, the code may be checked to determine whether it is functionally correct and/or run-time statistics may be collected regarding the program associated with the first processor.

40 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 12

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L10: Entry 1 of 2

File: USPT

Dec 7, 1999

US-PAT-NO: 5999734

DOCUMENT-IDENTIFIER: US 5999734 A

**** See image for Certificate of Correction ****

TITLE: Compiler-oriented apparatus for parallel compilation, simulation and execution of computer programs and hardware models

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Willis; John Christopher	Rochester	MN		
Newshutz; Robert Neill	Rochester	MN		

US-CL-CURRENT: 717/149; 709/200, 709/201, 712/1, 712/15, 712/28

ABSTRACT:

A distributed, compiler-oriented database is disclosed with operating modes including parallel compilation, parallel simulation and parallel execution of computer programs and hardware models. The invention utilizes a hardware apparatus consisting of shared memory multiprocessors, optionally augmented by processors with re-configurable logic execution pipelines or independently scheduled re-configurable logic blocks and a software database apparatus, manifest in the hardware apparatus, in order to efficiently support parallel database clients such as a source code analyzer, an elaborator, an optimizer, mapping and scheduling, code generation, linking/loading, execution/simulation, debugging, profiling, user interface and a file interface.



44 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 10

Freeform Search

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side by side			
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L14</u>	L13 and simulat\$6	5	<u>L14</u>
<u>L13</u>	static\$10 adj3 thread	79	<u>L13</u>
<u>L12</u>	single static\$10 adj3 thread	0	<u>L12</u>
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<u>L8</u>	dynamic\$6 adj3 allocat\$3 thread	1	<u>L8</u>
<u>L7</u>	simulat\$6 same dynamic\$6 adj3 allocat\$3 thread	0	<u>L7</u>
<u>L6</u>	simulat\$6 near5 dynamic\$6 adj3 allocat\$3 thread	0	<u>L6</u>
<i>DB=PGPB; PLUR=YES; OP=ADJ</i>			
<u>L5</u>	simulat\$6 near5 dynamic\$6 adj3 allocat\$3 thread and static\$10 adj3 allocated thread	0	<u>L5</u>
<u>L4</u>	L3	0	<u>L4</u>
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L3 simulat\$6 near5 dynamic\$6 adj3 allocat\$3 thread and static\$10 adj3
 allocated thread

0 L3

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L2 L1

0 L2

DB=USPT; PLUR=YES; OP=ADJ

L1 simultat\$6 near5 dynamic\$6 adj3 allocat\$3 thread and static\$10 adj3
 allocated thread

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